WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device comprising:

a semiconductor substrate having a main surface provided with two spaced trenches;

an isolation insulator filling said trench, said isolation insulator having an upper surface with an end having a curvature protruding toward said semiconductor substrate;

a floating electrode having a flat surface and extending from the main surface of said semiconductor substrate between said two trenches to said two isolation insulators;

an insulation film extending from the upper surface of said floating electrode to a side surface of said floating electrode overlying said isolation insulator; and

a control gate disposed on said insulation film to extend from the upper surface of said floating electrode to the side surface of said floating electrode.

2. The non-volatile semiconductor memory device according to claim 1, wherein a sidewall surface of said trench and the main surface of said semiconductor substrate underlying said floating electrode are connected together by a portion providing said semiconductor substrate with a curved surface.

3. The non-volatile semiconductor memory device according to claim 1, wherein as seen in a direction of a length of said floating electrode, said trench has a width smaller than a distance between said two trenches.

4. The non-volatile semiconductor memory device according to claim 1, said semiconductor substrate including a memory cell region having formed therein a memory cell including said floating electrode, said insulation film and said control electrode, and a peripheral circuitry region corresponding to a region other than said memory cell region, in said

peripheral circuitry region said semiconductor substrate having the main surface provided with another trench, the non-volatile semiconductor memory device further comprising another isolation insulator disposed in said another trench, wherein as seen in a direction substantially perpendicular to the main surface of said semiconductor substrate, said another isolation insulator arranged in said peripheral circuitry region is larger in thickness than said isolation insulator arranged in said memory cell region.

5. A method of fabricating a non-volatile semiconductor memory device, comprising the steps of:

providing a semiconductor substrate at a main surface with two spaced trenches;

providing in said trench an isolation insulator having a protrusion protruding upper than a main surface of said semiconductor substrate;

isotropically etching away said protrusion partially to reduce said protrusion to be smaller in width than said trench;

after the step of isotropically etching, providing said semiconductor substrate at the main surface with a conductor film extending from a region located between said two isolation insulators to said isolation insulator;

removing an upper surface layer of said conductor film to expose an upper portion of said isolation insulator to provide a floating electrode formed of said conductor film, having a flat upper surface and located between said isolation insulators; and

etching away the upper portion of said isolation insulator adjacent to said floating electrode to expose a side surface of said floating electrode.

6. The method according to claim 5, wherein:

the step of providing said semiconductor substrate at the main surface with said two spaced trenches includes the step of providing on the main surface of said semiconductor substrate a mask layer formed of stacked layers including a buffer conductor film layer, and having an open pattern positioned on a region to be provided with said two trenches, and the step of

anisotropically etching the main surface of said semiconductor substrate with said mask layer used as a mask to partially remove the main surface of said semiconductor substrate to form said two trenches, in said mask layer said buffer conductor film layer being partially exposed to a side surface defining said open pattern;

the step of providing said isolation insulator includes the step of thermally oxidizing a side surface of said two trenches with said mask layer in existence to provide a first oxide film forming said isolation insulator, and the step of providing a second oxide film forming said isolation insulator on said first oxide film to fill said two trenches; and

the step of isotropically etching away includes the step of removing said mask layer.

7. The method according to claim 5, wherein the step of providing said semiconductor substrate at the main surface with said two spaced trenches includes the steps of :

providing on the main surface of said semiconductor substrate a mask layer having an open pattern positioned on a region to be provided with said two trenches;

providing a sidewall film on a sidewall of said mask layer defining said open pattern;

with said mask layer and said sidewall film used as a mask, anisotropically etching the main surface of said semiconductor substrate away partially to provide said two trenches.

8. The method according to claim 5, said semiconductor substrate including a memory cell region provided with a memory cell having said floating electrode and a peripheral circuitry region corresponding to a region other than said memory cell region, comprising the steps of:

providing another trench in said peripheral circuitry region at the main surface of said semiconductor substrate; and

providing in said another trench another isolation insulator having a protrusion protruding upper than the main surface of said semiconductor

substrate, wherein in the step of etching away, said another isolation insulator underlying a protection film has the upper portion etched away.